PATENT APPLICATION

TRENCH TRANSISTOR WITH SUPERIOR GATE DIELECTRIC

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BACKGROUND OF THE INVENTION

The present invention relates in general to field effect transistors, and in particular trench transistors and methods of their manufacture.

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Figure 1 is a simplified cross section of a portion of a conventional metal-oxide-semiconductor field-effect transistor ("MOSFET") trench transistor. A trench 10 is lined with an electrically insulating material 12 that will act as a gate dielectric, and is filled with a conductive material 14, such as polysilicon, which forms the gate. The trench, and hence the gate, extend from the surface of

15 the silicon into the substrate down through a body region 22 (in this case a P-type region) and a drain region 16 (in this case an n-type region). Drain region 16 may be electrically contacted through the substrate of the device. N-type regions on either sides of trench 14 form source terminal 18 of the MOSFET. An active

20 channel region 20 is thus formed along side of trench 16 between source regions 18 and drain region 16.

Trench transistors are often used in power-handling applications, such as power management circuitry for a computer. Trench transistors often

25 operate at 5-100 V, as compared to 2-5 V for a logic-type MOSFET, and trench transistors may control up to 100 amps of current in some applications. Different operating conditions create different problems that must be addressed by proper design of the devices. For example, logic and other low-voltage MOSFETs typically do not have to withstand the voltage differentials that can appear across

the terminals of a trench transistor, such as between the gate and drain ("V_{GD}"). These high voltages can stress the gate oxide, causing breakdown and degradation leading to device failure.

5   The gate oxide of a conventional MOSFET is typically formed on a planar surface of a semiconductor wafer. Forming a high-quality oxide layer on a planar surface is relatively simple compared to forming a high-quality oxide layer in a trench for several reasons. One difficulty is that thermally grown oxide will grow faster on a flat surface than at a corner. Fig. 2 is a simplified cross section of 10 a portion of a silicon wafer 30 with a convex corner 32 and a concave corner 34. A layer of thermal oxide 36 is thinner at both the convex corner and at the concave corner. Further, because of higher stress at the silicon-oxide interface at the corners, the corner Si-O bonds are more strained and thus require lower energy to break them. The combination of the thinner oxide and the strained Si-O bonds at 15 the corners make the corner structure less resistant to breakdown at a given electric field across the gate oxide. As a result, the device may exhibit higher leakage currents and suffer related yield and reliability problems. The leakage and other reliability problems are exacerbated by the dry etch process that is typically used to form the trench. Dry etching leaves relatively rough trench walls and creates 20 dangling bonds that further contribute to the leakage.

    Thus, it is desirable to produce a trench transistor with a gate dielectric of more uniform thickness, and lower gate leakage current.

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SUMMARY OF THE INVENTION

    The present invention provides a trench metal oxide semiconductor field effect transistor (MOSFET) with a rugged gate dielectric layer which exhibits lower gate leakage current. Gate dielectric (e.g. oxide) is grown on the trench 30 walls and bottom at a temperature sufficiently high to reduce the viscosity of the

oxide during growth to result in an oxide layer of more uniform thickness. In one embodiment, the high-temperature oxide layer is grown at 1,100°C to a thickness of about 500 A thick and exhibits reduced gate leakage current and higher gate rupture voltage compared to a trench transistor with a gate oxide layer of similar thickness grown at the lower temperatures (e.g., 950°C) conventionally used in the industry. In a preferred embodiment, a gate dielectric layer is made from a first layer of high-temperature gate oxide, a layer of silicon nitride, and a second layer of gate oxide. This composite gate dielectric layer at optimized thicknesses results in even lower gate leakage current and higher gate rupture voltage.

Accordingly, in one embodiment, the present invention provides a field effect transistor formed on a silicon substrate, the transistor including a trench extending into the substrate, the trench having a gate oxide layer having been grown at a temperature above about 1,100 °C to result in the gate oxide layer having a thickness that is substantially uniform, the gate oxide layer having substantially uniform stress.

In another embodiment, the present invention provides field effect transistor formed on a silicon substrate, the transistor including a trench extending into the substrate, the trench being substantially filled by a conductive material that is separated from trench walls and bottom by a dielectric material, the dielectric material including: a silicon nitride layer sandwiched between a first oxide layer adjacent to the trench walls and bottom, and a second oxide layer adjacent to the conductive material, the first oxide layer having a thickness that is substantially greater than that of the second oxide layer.

The following detailed description and the accompanying drawings provide a better understanding of the nature and advantages of the trench transistor with rugged gate oxide according to the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified cross section of an exemplary conventional trench transistor;

5   Fig. 2 is a simplified cross section of a thermal oxide layer on a portion of a silicon wafer having a convex corner and a concave corner;

Fig. 3 is a diagram illustrating trench corners along longitudinal axis of an open cell trench transistor;

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Fig. 4 illustrates a composite oxide-nitride-oxide dielectric layer in greater detail for a trench transistor according to the present invention;

Fig. 5 is a graph of gate leakage current versus gate voltage for

15   various gate dielectric structures;

Fig. 6A is a simplified flow chart of a method for forming a gate dielectric oxide layer according to an embodiment of the present invention; and

20   Fig. 6B is a simplified flow chart of a method for forming a gate dielectric layer according to another embodiment of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

25   Trench transistors with superior gate dielectric layers can be fabricated by improving the consistency of the dielectric layer thickness, by reducing the stress in certain regions of the layer, and by improving the dielectric strength of the dielectric layer. These superior gate dielectric characteristics result in trench transistors with lower gate leakage currents and higher gate dielectric

30   rupture voltages, thus providing devices with both improved performance and

reliability.

As described in connection with Figure 2, in trench MOSFETs, the gate dielectric layer must typically cover concave and convex corners of the trench. Referring to Figure 3, the top of the trench has convex corners 32, while the bottom of the trench has concave corners 34. In some cases, gate material 38 (e.g. polysilicon) that substantially fills the trench may be etched below surface 40 of substrate 42. This forms a recess that eliminates the need for dielectric layer 36 to cover convex corners 32. However, in addition to the remaining concave corners 34, convex corners 48 are formed at the longitudinal end of the trench, all of which are potential weak spots in gate dielectric layer 36.

Leakage current and breakdown voltage at the concave corners of a trench transistor are influenced by several factors that are by and large negligible in the context of other known trench structures such as trench capacitors. The greater dielectric thickness and higher operating voltages of trench transistors render the corner thinning effects much more acute in the case of trench transistors. Figure 3 illustrates another problem with trench transistors that involves electric field crowding at the corners of the gate. When one voltage, V_G, is applied to the gate and a different voltage, V_D, is applied to the drain, an electric field is established through the gate oxide, represented by field lines 44. The field lines become crowded at the corners of the gate, intensifying the field gradient in this region. Unfortunately, this is the same region in which oxide thinning might occur, which can further increase the field gradient and lead to breakdown or leakage current.

Gate leakage current may occur by a variety or combination of mechanisms such as Fowler-Nordheim tunneling or trap-assisted tunneling. Several aspects of trench transistors might contribute to these or similar mechanisms resulting in greater gate leakage current. For example, thinner oxide

that may be present at the trench corners provides a lower barrier for carriers to overcome. Also, it is believed that the stress in a thinned oxide layer at a concave corner strains the Si-O bonds, allowing a carrier with less energy to break the Si-O bonds and overcome the dielectric barrier. It is further believed that the stress

5 forms trapping sites within the strained oxide layer, which allows easier transport of carriers through the oxide.

An artifact of the trench-forming process (e.g., dry etch) is that the trench wall has a surface that is rougher than the typical surface of a polished

10 silicon wafer. After the growth of an oxide layer on the rough surface, it is believed that a larger number of traps exist in the bulk oxide and a larger number of dangling bonds exist at the Si-O interface than would exist in an oxide layer formed on a conventional, polished silicon surface. Thus, some of the leakage current arises from conditions not normally found in conventional MOSFETs.

15 Unfortunately, gate leakage current can degrade the quality of the gate oxide, creating more traps and thus leading to more leakage current. The high-voltage, high-current operating conditions of trench transistors may accelerate this process by providing a large number of high-energy carriers.

20 Therefore, it is important that trench transistors have not only a uniform gate oxide layer, but that the layer be relatively stress-free, especially in the regions of high field gradients, such as at the corners of the gate. The present invention achieves this, in one embodiment, by growing the oxide layer at a temperature well above the temperatures used in conventional thermal oxidation

25 processes. For example, conventional thermal oxide processes take place at about 900-950 °C. At this temperature, a thin oxide of a few hundred Angstroms can be grown in a controllable amount of time, such as several minutes, but will exhibit corner thinning and have residual stress. According to the present invention, however, trench gate oxide is preferably grown at about 1,100 °C or higher,

30 resulting in substantially reduced corner thinning and substantially reduced

residual stress at the corners, as well. At this higher temperature the viscosity of the oxide decreases, allowing the oxide to flow laterally as it grows in response to the crowding stress at the corners. Thus, not only is thinning reduced, but the residual stress is also reduced. The resulting bulk silicon-oxide interface is also

5   smoother, because of the reduced stress and/or lateral flow. This interface smoothing also reduces carrier scattering and increases mobility in the channel region of the trench transistor. At such elevated temperatures, limited thermal budgets and rapid oxide growth can become problems if steps are not taken to address these effects. For example, rapid thermal processing (RTP) may be

10   employed to avoid exceeding the thermal budget allowed by the process flow. Also, partial pressure of oxygen in the furnace can be reduced to slow down oxide growth.

     Gate leakage current in trench MOSFETs is further reduced

15   according to the present invention by inserting an additional barrier layer in the gate dielectric material. Figure 4 illustrates a cross-sectional view of a composite oxide-nitride-oxide dielectric layer 110 for a trench transistor according to an embodiment of the present invention. According to this embodiment, trench gate dielectric layer 110 includes a first or outer oxide layer 100, a middle silicon

20   nitride layer 104, and a second or inner oxide layer 106. First oxide layer 100 is thermally grown to a thickness of, for example, 300 Å. In a preferred embodiment, first oxide layer 100 is grown at the higher temperature of 1,100 °C. The wafer may be preferably a (100) single-crystal silicon wafer with a nominal doping concentration of 1×10^{16} cm^{-3} using, e.g., Boron or Phosphorous.

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     Silicon nitride layer 104 is deposited using preferably a low-pressure chemical-vapor deposition ("LPCVD") process to form a layer of silicon nitride having an exemplary thickness of approximately 120 Å. The LPCVD process, as opposed to, e.g., CVD carried out at atmospheric pressure, provides good step

30   coverage that results in a conformal layer of uniform thickness to line the trench.

After depositing silicon nitride layer 104, inner thermal oxide layer 106 is grown to an exemplary thickness of approximately 50 Å. Inner oxide layer 106 promotes adhesion to gate polysilicon 108 and serves to balance stress between the silicon nitride layer and the gate oxide layer, and to serve as stress relief between the

5   silicon nitride layer and the polysilicon gate. The resulting gate dielectric structure 110, which includes the gate oxide layer 100, silicon nitride layer 104, and inner oxide layer 106, has an exemplary thickness of about 470 Å.

Figure 5 shows the gate leakage and gate rupture voltage for various

10   gate dielectric layers. A standard 500 Å gate oxide grown at 1000 °C is shown to have a gate leakage current I_{GSS} of about 10 nA at a V_{GSS} of 30 V, and a gate rupture voltage of about 38 V. By comparison, a gate oxide of the same thickness grown at a temperature of 1100 °C in accordance with the present invention has an I_{GSS} of about 4 nA at V_{GSS} = 30 V, and a gate rupture voltage of about 37.5 V. 610.

15   The oxide-nitride-oxide dielectric layer shown in Figure 4, which has a thickness equivalent to the gate oxide layers, has an I_{GSS} of only about 1 nA at V_{GSS}=30 V, and a surprisingly high gate rupture voltage of about 46 V.

The comparison between the gate leakage currents and gate rupture

20   voltages for gate oxide layers of trench transistors grown at conventional temperatures and grown according to the present invention shows that a superior gate dielectric layer is produced by growing the gate oxide layer at a temperature above about 1100 °C. Furthermore, the addition of a relatively thin layer of silicon nitride further improves the performance of the gate dielectric layer without

25   increasing the total thickness of the gate dielectric layer.

Figure 6A is a simplified flow chart of a method 701 of manufacturing a gate oxide layer according to an embodiment of the present invention. A trench is formed in a silicon substrate (step 703). A thermal oxide

layer is then grown at a temperature above about 1100 °C to a thickness of at least about 100 A (step 705) to line the trench.

5   Figure 6B is a simplified flow chart of a method 702 of manufacturing a gate dielectric layer according to another embodiment of the present invention. A trench is formed in a silicon substrate (step 703) and a thermal oxide layer is grown at a temperature of above about 1000°C, and preferably at 1100°C, to a thickness of at least about 100 A (step 705) to line the trench. A layer of silicon nitride is formed over the thermal oxide layer (step 707),

10   such as by LPCVD, and a second layer of silicon oxide is formed over the silicon nitride (step 709).

While the above is a complete description of specific embodiments of the present invention, various modifications, variations, and alternatives may be

15   employed. For example, although LPCVD has shown to produce a uniform, conformal layer of silicon nitride, other deposition processes may produce suitably uniform layers within a trench, depending on the trench geometry. Alternatively, a composite gate dielectric layer may be formed by nitriding the gate oxide layer, either before or during thermal oxide growth. Similarly, although a gate dielectric

20   layer 500 A thick was given as a specific example, thicker or thinner gate dielectric layers may be appropriate according to the design of the device. Therefore, the scope of this invention should not be limited to the embodiments described, and should instead be defined by the following claims.